FORM PTO-1390 (REV. 1-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
09/623646

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/GB99/00695	**08 March 1999 (08.03.1999)**	**06 March 1998 (06.03.1998)**

TITLE OF INVENTION
PREDISTORTER

APPLICANT(S) FOR DO/EO/US
KENNINGTON, Peter

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 37 (b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)) (unexecuted)
10. ☐ Amendments made to the International Application under PCT Article 34(2)(b)
11. ☐ An Information Disclosure Statement under 37 CFR 1.197 and 1.98
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: Express Mail Procedure under 37 C.F.R. § 1.10

I hereby certify that this Transmittal Letter to the United States Designated/Elected Office (DO/EO/US) Concerning a Filing under 35 U.S.C. 3.71, along with any paper referred to as being attached or enclosed, is being deposited with the United States Postal Service on the 6th day of September 2000 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR 1.10, Mailing Label Number EL602995655US addressed to the Box PCT, Assistant Commissioner for Patents, Washington, D.C. 20231.

Odessa Roberts
Signature

533 Rec'd PCT/PTO 06 SEP 2000

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/623646	PCT/GB99/00695	

17. ☒ The following fees are submitted

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):		CALCULATIONS PTO USE ONLY
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	$970.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO	$840.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2) paid to USPTO	$690.00	
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$670.00	
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4)	$96.00	

ENTER APPROPRIATE BASIC FEE AMOUNT =				$ 840.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$ 130.00	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	18 - 20 =	0	X $18.00	$ 0.00	
Independent claims	3 - 3 =	0	X $78.00	$ 0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+$260.00	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$ 970.00	
Reduction of ½ for filing by small entity, if applicable. A Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) --				$ -485.00	
SUBTOTAL =				$ 485.00	
Processing fee of $130.00 for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$ 0.00	
TOTAL NATIONAL FEE =				$ 485.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40 per property				$ 0.00	
TOTAL FEES ENCLOSED =				$ 485.00	
				Amount to be refunded:	$
				charged:	$

a. ☐ A check in the amount of $1100.00 to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 11-0855 in the amount of $485.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-0855. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b) must be filed and granted to restore the application to pending status.

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CUSTOMER NUMBER BAR CODE LABEL:

23370

PATENT TRADEMARK OFFICE

Geoff L. Sutcliffe
SIGNATURE

Name: Geoff L. Sutcliffe
Registration No. 36,348

STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(c))--SMALL BUSINESS CONERN

Docket Number (Optional)

Applicant , Patentee, or Identifier:	Peter Kenington
International Application No.	PCT/GB99/00695
Filed:	March 8, 1999
Title:	Predistorter

I hereby state that I am

the owner of the small business concern identified below

an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Small Business Concern: Wireless Systems International Limited

Address of Small Business Concern: Innovation House
Bristol Business Park
Coldharbour Lane
Bristol BS16 1EJ United Kingdom

I hereby state that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR Part 121 for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of the employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time, or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby state that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention described in:

the specification filed herewith with title as listed above.

the application identified above.

the patent identified above

If the rights held by the above-identified small business concern are not exclusive, each individual, concern, or organization having rights in the invention must file separate statements as to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern, or organization having any rights in the invention is listed below:

no such person, concern, or organization exists.

each such person, concern, or organization is listed below.

Name of Small Business Concern

Address of Small Business Concern

Separate statements are required from each named person, concern, or organization having rights to the invention stating their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

Name of Person Signing PETER B. KENINGTON

Title of Person if other than Owner CHIEF TECHNOLOGY OFFICER

Address of Person Signing TRAP FARM, DEVAUDEN, CHEPSTOW NP6 6PE, UK

Signature P.B. Kenington Date 6th FEBRUARY 2001

IN THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

Applicant:	KENNINGTON, Peter	
International Application No.:	PCT/GB99/00695	Express Mail Label No. EL602995655US
International Filing Date:	08 March 1999	Date of Deposit: 06 September 2000
Title:	PREDISTORTER	

Box PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Please preliminarily amend the national phase entry of the above-identified application as follows:

In the Claims

Please delete claims 1-18 and insert the following new claims:

--19. A circuit for deriving a third order signal from an input signal, comprising input circuitry for providing an input signal to the circuit along first, second and third paths, a first combiner for combining the input signal from the first and second paths to produce a second order signal on a squared signal path, a filter for low-pass filtering the second order signal to remove components at the frequency of the input signal and harmonics thereof, and a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce a third order signal.

20. A circuit as claimed in claim 19, for additionally deriving a fifth order signal from an input signal, further comprising circuitry for providing the second order signal along a second squared signal path, and a third combiner for combining the second order signal from the second squared signal path with the third order signal to produce a fifth order signal.

21. A circuit as claimed in claim 19, for additionally deriving a fifth order signal from an input signal, wherein the input circuitry provides the input signal along fourth and fifth paths, and further comprises a third combiner for combining the input signal from the fourth path with the third order signal to produce a fourth order signal, and a fourth combiner for combining the input signal from the fifth path with the fourth order signal to produce a fifth order signal.

22. A circuit as claimed in claim 19, wherein the input signal is a radio frequency signal.

23. A circuit as claimed in claim 19, further comprising an injector for injecting a direct current signal into at least one of the signal paths.

24. A circuit as claimed in claim 23, wherein the injector is arranged to inject the direct current signal into the squared signal path for adding to the second order signal to cancel input signal energy in the third order signal.

25. A circuit as claimed in claim 24, further comprising an error corrector arranged to compare the third order signal with the input signal to produce an error correction signal for controlling the injection of the direct current signal into the squared signal path.

26. A circuit as claimed in claim 25, wherein the error corrector is arranged to translate the frequency of the third order signal by an oscillator signal prior to correlation with the input signal to produce a correlation signal which is processed in a digital signal processor by comparison with the oscillator signal to produce the error correction signal.

27. A circuit as claimed in claim 23, further comprising an injector for injecting the direct current signal into the second squared signal path for adding to the second order signal to cancel input signal energy and third order signal energy in the fifth order signal.

28. A circuit as claimed in claim 25, further comprising an error corrector arranged to compare the fifth order signal with the third order signal to produce an error correction signal for controlling the injection of the direct current signal into the second squared signal path.

29. A circuit as claimed in claim 19, wherein the combiners are selected from mixers and multipliers.

30. A circuit as claimed in claim 19, wherein the input circuitry comprises at least one splitter for providing the input signal along the signal paths.

31. A circuit as claimed in claim 19, wherein the input circuitry comprises at least one directional coupler for providing the input signal along the signal paths.

32. A polynomial predistorter including a circuit for deriving a third order predistortion signal from an input signal, comprising input circuitry for providing an input signal to the circuit along first, second and third paths, a first combiner for combining the input signal from the first and the second paths to produce a second order signal on a squared signal path, a filter for low-pass filtering the second order signal to remove components at the frequency of the input signal and harmonics thereof, and a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce a third order signal.

33. A method of deriving a third order predistortion signal from an input signal, comprising providing an input signal to a circuit along first, second and third paths, combining the input signal from the first and second paths to produce a second order signal on a squared signal path, low-pass filtering the second order signal to remove components at the frequency of the input signal and harmonics thereof, and combining the filtered second order signal from the squared signal path with the input signal from the third path to produce a third order signal.

34. A circuit as claimed in claim 19, further comprising a generator for creating at least one further, different, odd-order signal, each said distinct, further odd-order signal being created by combining the input signal with itself.

35. A polynomial predistorter according to claim 32, further comprising a generator for creating at least one further, different, odd-order signal, each said distinct, further odd-order signal being created by combining the input signal with itself.

36. A method according to claim 33, further comprising creating at least one further, different, odd-order signal, each said distinct, further odd-order signal being created by combining the input signal with itself.

Respectfully submitted,

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Date: 06 September 2000
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PREDISTORTER

This invention relates to a circuit for deriving a third order signal from an input signal. In particular, the invention relates to a circuit for use in a polynomial predistorter.

In an ideal system, a linear amplifier provides uniform gain throughout its dynamic range in order that the output signal of the amplifier is a correct, amplified version of the input signal. In reality however all linear amplifiers exhibit non-ideal properties such as amplitude and phase distortion, which are undesirable and can seriously deteriorate the performance of a system. One effect of this non-linearity of the amplifier is the generation of output frequencies equal to the sums and differences of integer multiples of the input frequency components. This effect is known as intermodulation distortion (IMD) and is particularly undesirable in high-power radio frequency (RF) amplifiers designed for use in broadband systems. For example, a broadband amplifier used in the TDMA cellular system will generate various intermodulation products as a result of amplifying a multitude of TDMA channels occurring at fixed frequency intervals across a TDMA band, with coincident active frames.

A number of linearisation techniques have been developed to overcome the above distortion problems associated with a linear amplifier. A few of these techniques operate in real-time to account for time dependent changes in the non-linear characteristics of the amplifier. Such changes may result from, for example, temperature variations in the amplifier, aging of amplifier components, power supply fluctuations, or, most importantly, the input carriers. Of the broadband, RF-based linearisation techniques, the two most commonly used are feed forward linearisation and predistorter linearisation.

A feed forward linearisation mechanism relies on creating an error signal representative of the IMD products introduced by the linear amplifier, and feeding this signal forward to combine with the output spectrum of the amplifier, cancelling out the unwanted distortion. In order for the cancellation process to operate correctly, it is necessary for the mechanism to accurately adjust the amplitude and phase of the error signal prior to combining it with the output of the amplifier. This typically involves the use of additional amplifiers and lossy delay lines and couplers appearing in the output path from the main amplifier. These losses and the requirement for additional amplifiers, which are not adding to the output power of the system, result in a low-efficiency solution.

In general, predistortion linearisation mechanisms involve deliberate alteration of the relatively low level input signal to the amplifier in anticipation of the undesired distortion process occurring within the amplifier. Specifically, the mechanism predistorts the input signal in a inverse sense to the distortion produced by the amplifier such that in series the overall distortion is minimised. Accordingly, the transfer characteristic of the predistorter is approximated as closely as possible to the inverse or complementary function of the transfer characteristic of the amplifier. If the linear amplifier is compressive, i.e. the gain tails off at higher power levels, then the predistorter will compensate for this compression by correspondingly expanding the input signal.

Several approaches exist for predistorting the input signal, each differing in the way the predistorter approximates the inverse or complementary function. One approach approximates the inverse function with the exponential characteristics of a diode. One or

more diodes may be used together with appropriate biasing to achieve a reduction of the distortion in the order of 10 dB. A second approach is to perform a piece-wise approximation of the inverse function using a series of linear gain, straight line elements interconnected end-to-end. A drawback with this approach is that the alignment and control of the line elements requires complex circuitry owing to the interconnection points having two degrees of freedom.

Polynomial predistortion is another approach to approximating the inverse function of the amplifier transfer characteristic. It is based on a polynomial expansion of the inverse function which may be expressed as follows:

$$y = a + bx + cx^2 + dx^3 + ex^4 + fx^5 + gx^6 + hx^7....$$

The term a is an offset which may be set to zero in a practical polynomial predistorter. The term bx represents the gain of the predistorter which is linear and merely contributes to the gain of the main amplifier. The terms containing even powers of x represent harmonic distortion components generated in the main amplifier which may be removed using frequency filtering, and therefore these terms may also be set to zero. The remaining terms containing odd powers of x represent in-band distortion caused by the main amplifier (in addition to harmonics which can be filtered as above). In fact, each of these odd-power terms may be considered to represent the equivalent order of intermodulation distortion generated in the main amplifier.

According to a first aspect of the present invention there is provided a circuit for deriving a third order signal from an input signal, comprising input means for providing an input signal to the circuit along first, second and third paths, means for combining the input signal from the first and second paths to produce a second order signal on a squared signal path, means for low-pass filtering the second order signal to remove components at the frequency of the input signal and harmonics thereof, and means for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce a third order signal.

A circuit in accordance with the first aspect of the present invention provides the advantage that the third order signal generation may take place using relatively low frequency technology to combine the second and first order signals. The generation of second and third order signals may also enable the generation of higher-order terms of distortion component such as fifth or seventh order.

Ideally, the input signal is a radio frequency (RF) signal which may contain a plurality of channels across a signal bandwidth.

In a first embodiment in accordance with the invention, the third order signal is provided as a third order distortion component at an output of the circuit.

In a second embodiment in accordance with the invention, the circuit further comprising means for providing the second order signal along a second squared path, and means for

combining the second order signal from the second squared path with the third order signal to produce a fifth order signal.

In a third embodiment in accordance with the invention, the circuit is for deriving a fifth order signal from an input signal, whereby the input means provides the input signal along fourth and fifth paths, and further comprises means for combining the input signal from the fourth path with the third order signal to produce a fourth order signal, and means for combining the input signal from the fifth path with the fourth order signal to produce a fifth order signal.

A similar approach may be used in the generation of a seventh order distortion component at an output of the circuit.

The third order signal may contain input signal energy. Similarly, the fifth order signal may contain both input signal energy and third order signal energy.

In a preferred embodiment of the invention, the circuit further comprising means for injecting a direct current (DC) signal either directly into at least one of the signal paths and/or into at least one of the means for combining the signals. Depending on the injection position, the effect of the DC signal is to remove input signal energy from the third order signal, or to remove input signal energy and third order signal energy from the fifth order signal.

In the first embodiment, the DC signal is ideally injected into the squared path to add to the second order signal. The DC signal may also be injected in the first, second or third paths to achieve the same effect.

In the second embodiment, the DC signal is ideally injected into the second squared path to add to the second order signal.

The DC injection may be controlled (maintained) by an error correction or feedback loop. Suitably, the feedback loop is arranged so as to optimise removal of unwanted signal energies which occur in the third and fifth order signals.

Preferably, the feedback loop makes use of digital signal processing (DSP) techniques to reduce the effect of DC offsets produced by analogue components.

Preferably, the means for combining may be a mixer or a multiplier, and the means for providing a signal along more than one path may include at least one splitter for splitting an incoming signal.

Further features and advantages of the invention will be apparent from the description below.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a multiple-order polynomial predistorter;

Figure 2 is a block diagram of a circuit for generating a third order distortion component suitable for use in the polynomial predistorter of Figure 1;

Figure 3 is a block diagram of a feedback control circuit for use in the circuit of Figure 2;

Figure 4 is a block diagram of an enhanced feedback control circuit using digital signal processing techniques for use in the circuit of Figure 2;

Figures 5 is a block diagram of a circuit for generating third and fifth order distortion components suitable for use in the polynomial predistorter of Figure 1;

Figure 6 is a block diagram of an alternative circuit for generating third and fifth order distortion components suitable for use in the polynomial predistorter of Figure 1;

Figure 7 is a block diagram of a circuit for generating a fifth order distortion component, based on the circuit of Figure 5 and including a feedback control circuit;

Figure 8 is a block diagram of a circuit for generating third and fifth order distortion components, based on the circuits of Figure 2 and Figure 7 and including a feedback control circuit ;

Figure 9 is a block diagram of a feedback control circuit for use in the circuit of Figure 8, based on the circuit of Figure 4;

Figure 10 is a block diagram of a circuit for generating third, fifth, and seventh order distortion components suitable for use in the polynomial predistorter of Figure 1; and

Figures 11a, 11b, 11c, 11d, 11e, 11f are frequency spectra for signals occurring at various points in the circuits of Figures 1 to 10 in operation.

Referring to Figure 1, there is shown a multiple order polynomial predistorter 200 having an input for receiving an RF input signal and an output for supplying a predistorted signal to an RF power amplifier 100. The RF input signal received at the input of the predistorter is split by the splitter 205 between two channels or paths, the main path 210 supplying the main RF input signal for subsequent amplification, and the distortion path 215 supplying multiple orders of distortion for adding to the main RF input signal.

The main RF input signal from the main path 210 and the distortion signal from the distortion path 215 are summed in the adder 220 prior to being amplified in the RF power amplifier 100. The main path includes a time delay component 225 to ensure that the main RF signal and the distortion signal coincide at the adder 220. In an ideal operation of the predistorter, the output signal from the RF power amplifier 100 will represent a linearly amplified version of the RF input signal as discussed previously. An example of a possible RF input signal in the form of two closely spaced frequency tones is shown in Figure 11a.

The RF signal entering the distortion path 215 is fed into a distortion generation circuit 230 which operates on the RF input signal to generate a set of non-linear distortion components each corresponding to a particular order of distortion. In Figure 1, the orders of distortion

generated at the three output paths of the distortion generation circuit 230 are third order, fifth order, and seventh order, illustrated as frequency spectra in Figures 11b, 11c and 11d respectively. It is also possible for the distortion generation circuit to generate higher order distortion components such as ninth order, or to generate only third order, or third and fifth order distortion components.

The signals output from the distortion generating circuit 230 are independently adjusted in phase by the set of variable phase-shift components 235 to compensate for any differing phase shifts occurring in the distortion generating circuit 230. The distortion signals are then independently adjusted in amplitude by the set of variable attenuators 240. The amplitude adjustment ensures that the relative levels of the separate distortion components are set to correctly correspond to the relative levels of the orders of distortion generated intrinsically in the RF power amplifier 100.

The correctly adjusted signals representing the third, fifth and seventh orders of distortion are then summed in the adder 245 to produce a single multiple order distortion signal. This signal is fed into an RF amplifier 250 which controls the level of the multiple order distortion signal relative to the main RF signal on the main path 210.

Figure 2 shows a block diagram of a circuit for generating a third order distortion component. The RF input signal entering the circuit is split three ways by the splitter 405. One of the RF signals is then fed into the first input of a mixer or multiplier 410 via a directional coupler 415. The directional coupler samples a portion of the RF signal which is fed into the second input of the mixer 410 via an attenuator 420. By mixing the two

versions of the same RF input signal, the output of the mixer 410 ideally generates a squared RF signal which contains frequency components in a DC zone, i.e. at low frequencies, and frequency components in a first harmonic zone, i.e. at double the original frequencies. The frequency spectra of the squared RF signal is represented in Figure 11e.

The squared RF signal output from the mixer 410 is then fed into the first input of a mixer 425 via an attenuator 430 and a DC injection summer 435. Another RF input signal from the splitter forms the second input to the mixer 425 and may be supplied via a path 440 including a time delay element (not shown) to ensure that the two mixer input signals are in phase. By mixing the squared RF signal with the original RF input signal, the output of the mixer 425 ideally produces a pure cubic signal. The frequency spectra of the cubed RF signal is represented in Figure 11f (after filtering to eliminate the DC-zone, harmonic and third harmonic components)

The cubed RF signal should, ideally, consist of only input RF signal energy, plus in-band third-order components. In practice however other higher orders of in-band distortion will also be present in the output of the mixer 425, together with more input signal energy than would be expected from a theoretical analysis. The attenuation values for the attenuators 420 and 430, and the coupling factor for the coupler 415 are chosen to optimise performance with the type of mixers 410 and 425. Optimum performance is a compromise between minimising the unwanted input signal energy, caused by leakage through the mixers, and minimising the higher orders of in-band distortion, caused by non-ideal performance of the mixers 410 and 425. In a circuit having a 0 dBm RF input signal level

and implementing standard Gilbert-cell based silicon IC mixers, the difference between the "LO", "RF" or "IF" drive levels will typically be in the order of 20 dB in each case.

In the third order distortion generator circuit of Figure 2, the squared RF signal output from the mixer 410 is filtered before entering the mixer 425. This enables selection of either the DC zone frequency components of the squared RF signal by means of a low pass filter (as illustrated: LPF432), or the second harmonic zone frequency components of the squared RF signal by means of a high pass filter. Each selection scheme has its own particular benefits, however, both schemes advantageously provide attenuation of the input tone energy at the output, when used in conjunction with the DC-based input tone rejection mechanism described below.

In the low pass filter version (note that protection is claimed only for apparatus and methods using such low-pass filtering), the selection of the DC zone in practice provides a better behaved response in terms of gain and phase flatness than the second harmonic zone and as a result can provide better coherence between the two third order distortion components shown in Figure 11b. Although the gain and phase flatness of the second harmonic zone version is effected by the high frequency response of the circuit elements, this version has the benefit of producing a output spectrum in which the input tone level is at a similar level to the third order distortion components, without additional correction.

In order to enable improved control of the third order component generation, it is preferable to remove as much of the input tone energy present in the output as possible. Referring to the circuit of Figure 2, this is achieved by injecting a DC signal via an adder 435 to the squared RF signal at an appropriate level such that when mixed with the RF

input signal the input energy at the output of the circuit is cancelled. The position of the DC signal injection shown in Figure 2 is preferable as the level of RF input to the mixer 425 is relatively high and is known to a high degree of certainty. The same cancellation of the input energy can however be achieved, albeit less efficiently and less predictably, by injecting a DC signal at other positions in the distortion generation circuit. For example, an alternative position for DC injection could be into the path 440 carrying the RF input signal to the mixer 425. The DC signal would then cancel any leakage of a spurious RF input signal present in the squared RF signal resulting from leakage through the mixer 410. DC signal injection may also be possible in the signal paths leading to the mixer 410.

Although the DC signal level may be set to maximise cancellation of the input signal energy in the output of the distortion generating circuit, fluctuations and drifting of the various signals within the circuit will occur as a result of, for example, temperature variations of circuit components, aging of circuit components, and unpredictable variations in supply voltages (see earlier comment on input signal levels). The distortion generation circuit therefore includes an automatic control mechanism 445 for initialising, maintaining, and controlling the DC signal at the correct level for maximum cancellation of the input signal energy. The automatic control mechanism operates using a feedback loop principle. The output of the distortion generation circuit is sampled by a splitter 450 and is fed into an input of the control mechanism. A second input of the control mechanism receives an RF input signal from the splitter 405, preferably via a time delay element (not shown), and functions as a reference signal for the RF input. The automatic control mechanism compares the sample from the output with the RF input reference signal, and provides as an

output a DC signal level dependent on the level of RF input energy detected in the output sample.

Figure 3 shows one implementation of the automatic control mechanism in which a detection mixer 455 receives at one input the sample of the output signal and at another input the reference input signal. The detection mixer outputs a signal containing components across a range of frequencies. However, the output of the detection mixer of interest is the DC signal component, which provides a measure of the overlap of the unwanted input signal energy in the output with the reference input signal. This DC output is isolated from the other signal components in the detection mixer output by integration of the output in the integrator 460. The integrator has a time constant long enough to remove the unwanted non-DC signal components but short enough to provide millisecond response in the feedback. The DC output of the integrator provides the DC signal for injection into the adder 435.

A drawback with this control mechanism is that the detection mixer and the integrator may generate DC offset signals which become dominant over the feed back control DC signals. This typically occurs when the level of rejection of the input energy is in the order of 10 - 15 dB. It is possible to use more accurate mixers and integrators to achieve lower DC offsets to counteract this effect. However, mixers and integrators of this kind tend to be rarer and more expensive.

Figure 4 shows a modified automatic control mechanism which incorporates offset frequency and digital signal processing (DSP) techniques to eliminate the DC offset problem referred to above. Although the circuit is more complex than the circuit of Figure

3, integration of the non-DSP components on an application specific integrated circuit (ASIC) chip means that the higher component count should not add significantly to the cost of this solution. The automatic control mechanism includes the same two inputs and one output as the circuit of Figure 3, and operates as follows. A low frequency (LF) fixed oscillator 465 operating in the digital domain of a digital signal processor (DSP) 470 provides via a digital-to-analogue converter 475 a low frequency tone signal to an input of a mixer 480. The LF tone signal is ideally at an audio frequency f_{LF} of between 1 and 5 kHz. The second input to the mixer 480 is the output sample supplied by the splitter 450 shown in Figure 2, and contains signal components at a relatively higher frequency than the LF tone signal, e.g. between 500 to 2000 MHz. The effect of mixing the output sample with the LF tone signal is to generate an image of the output sample shifted down in frequency by f_{LF} and an image of the output sample shifted up in frequency by f_{LF}. The output of the mixer 480 is processed by a high pass filter 485 which has a cutoff frequency chosen such that the filter 485 removes any LF tone signal leaking through the mixer 480. The frequency offset output sample is then fed into an input of a detection mixer 490, whilst a second input receives the reference RF input signal. As in the mechanism of Figure 3, the detection mixer 490 provides at its output a signal containing components across a range of frequencies. However, in this mechanism it is the signal component at the tone frequency f_{LF} which provides a measure of the overlap of the unwanted input signal energy in the output with the reference input signal.

After converting the output of the detection mixer 490 back into the digital domain of the digital signal processing (DSP) using the analogue-to-digital converter 495, the signal is fed into a digital mixer 500. It should be noted that the digital signal processor and the

analogue-to digital converter are ideally suited to dealing with signals at audio frequency and can therefore accurately process the required signal component at the tone frequency f_{LF}. The digital mixer 500 mixes the output of the detection mixer 490 with the LF tone signal from the LF fixed oscillator 465 to convert the required signal component also at the tone frequency to a DC signal. As in the mechanism of Figure 3, this DC signal is isolated from the other signal components produced in the detection mixer by integration of the digital mixer output in a digital integrator 505. However, unlike the mechanism of Figure 3, this offset-frequency mechanism is immune to any build up of spurious DC signals in the analogue domain, i.e. in the mixers 480, 490, the D/A 475, the A/D 495 and the high-pass filter 485. The potentially damaging DC signals enter the digital signal processor via the analogue to digital converter (A/D) 495, but are immediately converted to the tone signal frequency f_{LF} by the digital mixer 500 and are subsequently cancelled in the integrator 505. Because the digital mixer 500 and the integrator 505 both operate in the digital domain of the digital signal processor (DSP) they do not experience the problems of their analogue counterparts such as signal leakage or spurious DC offset generation due to temperature or power supply fluctuations. The DC signal output from the integrator provides via the digital-to-analogue converter 510 the DC signal for injection into the adder 435 of Figure 2.

Figures 5 and 6 are block diagrams of two alternative embodiments of a circuit for generating third and fifth order distortion components, and are based on the design and basic principles of operation of the third order generation circuit of Figure 2. Like components have therefore been labelled with like references.

In the generation circuit of Figure 5, the second order signal is divided into a second path 515 by a splitter 520, and the third order signal is divided into a second path 525 by a splitter 530. The second order signal level on the path 515, and the third order signal level on the path 525, are adjusted by an RF amplifier 535 and an attenuator 540 respectively. The adjusted second and third order signals are then mixed in the mixer 545 to produce a fifth order RF output. A second DC injection signal is added to the second order signal path 515 for mixing with the third order signal on the path 525. By adjusting the second DC signal to a suitable level, the third order signals, which would otherwise be present in the fifth order RF output, may be cancelled.

In the generation circuit of Figure 6, the RF input signal is further divided by a splitter 550 into paths 555 and 560, and the third order signal is divided by a splitter 530 into a path 525. The third order signal is suitably attenuated by attenuators 565 and 570 which in turn feed the mixers 575 and 580. The mixers 575 and 580 mix the third order signal with the RF input signals on the paths 555 and 560 respectively. The output of the first mixer 575 generates a fourth order signal, and the output of the second mixer 580 generates the fifth order distortion signal for outputting.

Simulations performed on the generation circuit of Figure 5 have shown that for fifth order distortion generation the first DC injection (DC1) to the adder 435 may not be required. The third DC injection can provide significant cancellation of both the main signal energy and the third order energy leaving only the desired fifth order distortion. Removal of the first and second DC injections allow for simpler control of the fifth order distortion

generation, however, a drawback in this solution is that the third order output no longer contains a pure third order distortion signal.

Figure 7 shows the circuit of Figure 5 with a feedback control mechanism which controls and maintains the second DC injection to the adder. This feedback control mechanism performs in a similar way as in the third order generation circuit, except that a sample of the fifth order output is compared with a reference signal sampled from the third order output. The feedback DC signal therefore provides a measure of the overlap of both the unwanted input signal energy and third order signal energy in the fifth order output. The feedback control mechanism may be implemented using the feedback circuits of Figures 3 or 4.

Figure 8 is a block diagram showing a third order and a fifth order distortion generation circuit with a combined control. The circuit is a combination of the third order generation circuit of Figure 2 and the fifth order generation circuit of Figure 7. The combined feedback control mechanism for this circuit is shown in Figure 9 and is based on the offset frequency mechanism of Figure 4.

Figure 10 is a block diagram showing a circuit for generating a seventh order distortion signal based on the principle used in the fifth order generation circuit of Figure 5. The fifth order signal is combined with the second order signal to generate a seventh order distortion output.

It will be evident in view of the foregoing that various modifications may be made within the scope of the present invention. For example, the description refers to the use of certain components such as mixers and integrators which could be replaced by multipliers and low-pass filters respectively.

Claims

1. A circuit for deriving a third order signal from an input signal, comprising input means for providing an input signal to the circuit along first, second and third paths, means for combining the input signal from the first and second paths to produce a second order signal on a squared signal path, means for low-pass filtering the second order signal to remove components at the frequency of the input signal and harmonics thereof, and means for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce a third order signal.

2. A circuit as claimed in claim 1, for additionally deriving a fifth order signal from an input signal, further comprising means for providing the second order signal along a second squared signal path, and means for combining the second order signal from the second squared signal path with the third order signal to produce a fifth order signal.

3. A circuit as claimed in claim 1, for additionally deriving a fifth order signal from an input signal, wherein the input means provides the input signal along fourth and fifth paths, and further comprises means for combining the input signal from the fourth path with the third order signal to produce a fourth order signal, and means for combining the input signal from the fifth path with the fourth order signal to produce a fifth order signal.

4. A circuit as claimed in any one of the preceding claims, wherein the input signal is a radio frequency signal.

5. A circuit as claimed in any one of the preceding claims, further comprising means for injecting a direct current signal into at least one of the signal paths.

6. A circuit as claimed in claim 5, wherein the d.c injecting means is arranged to inject the direct current signal into the squared signal path for adding to the second order signal to cancel input signal energy in the third order signal.

7. A circuit as claimed in claim 6, further comprising error correction means arranged to compare the third order signal with the input signal to produce an error correction signal for controlling the injection of the direct current signal into the squared signal path.

8. A circuit as claimed in claim 7, wherein in the error correction means is arranged to translate the frequency of the third order signal by an oscillator signal prior to correlation with the input signal to produce a correlation signal which is processed in a digital signal processor by comparison with the oscillator signal to produce the error correction signal.

9. A circuit as claimed in claim 5, further comprising means for injecting the direct current signal into the second squared signal path for adding to the second order signal to cancel input signal energy and third order signal energy in the fifth order signal.

10. A circuit as claimed in claim 7, further comprising error correction means arranged to compare the fifth order signal with the third order signal to produce an error correction signal for controlling the injection of the direct current signal into the second squared signal path.

11. A circuit as claimed in any one of the preceding claims, wherein the combining means are mixers or multipliers.

12. A circuit as claimed in any one of the preceding claims, wherein the input means comprises at least one splitter for providing the input signal along the signal paths.

13. A circuit as claimed in any one of the preceding claims, wherein the input means comprises at least one directional coupler for providing the input signal along the signal paths.

14. A polynomial predistorter including a circuit for deriving a third order predistortion signal from an input signal, comprising input means for providing an input signal to the circuit along first, second and third paths, means for combining the input signal from the first and the second paths to produce a second order signal on a squared signal path, means for low-pass filtering the second order signal to remove components at the frequency of the input signal and harmonics thereof, and means for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce a third order signal.

15. A method of deriving a third order predistortion signal from an input signal, comprising providing an input signal to a circuit along first, second and third paths, combining the input signal from the first and second paths to produce a second order signal on a squared signal path, low-pass filtering the second order signal to remove components at the frequency of the input signal and harmonics thereof, and combining the filtered second order signal from the squared signal path with the input signal from the third path to produce a third order signal.

16. A circuit as claimed in any one of claims 1 to 13, further comprising means for creating at least one further, different, odd-order signal, each said distinct, further odd-order signal being created by combining the input signal with itself.

17. A polynomial predistorter according to claim 14, further comprising means for creating at least one further, different, odd-order signal, each said distinct, further odd-order signal being created by combining the input signal with itself.

18. A method according to claim 15, further comprising creating at least one further, different, odd-order signal, each said distinct, further odd-order signal being created by combining the input signal with itself.

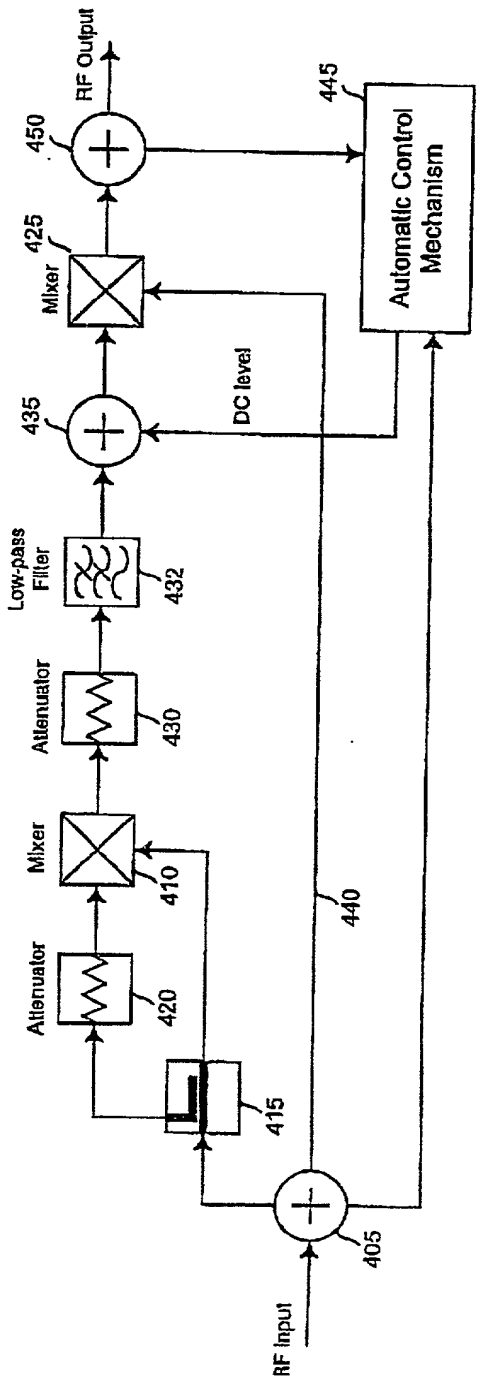

Figure 2

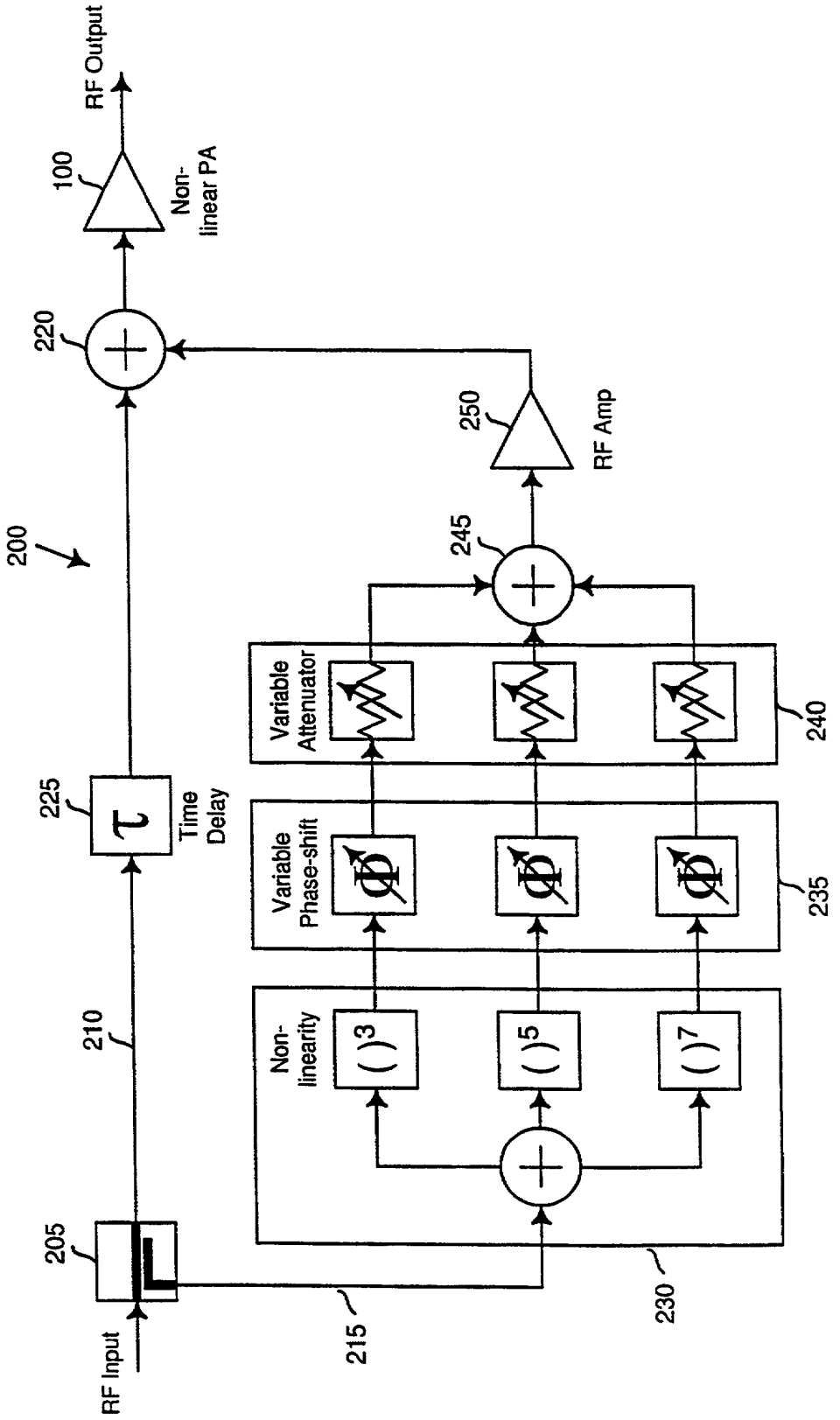
RF Output
100
Non-linear PA
220
250
RF Amp
200
245
Variable Attenuator
240
225
τ
Time Delay
Variable Phase-shift
235
210
Non-linearity
( )3
( )5
( )7
205
215
230
RF Input

Fig. 1

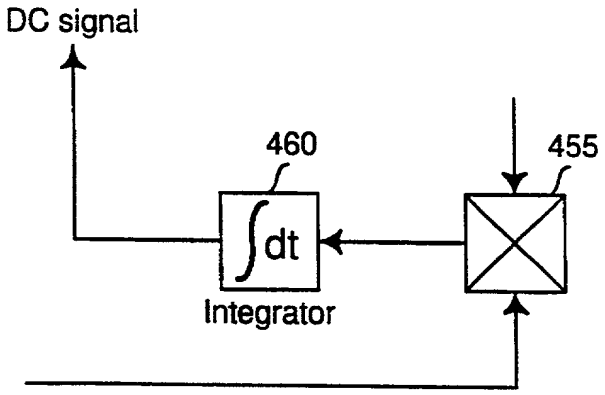

Fig. 3

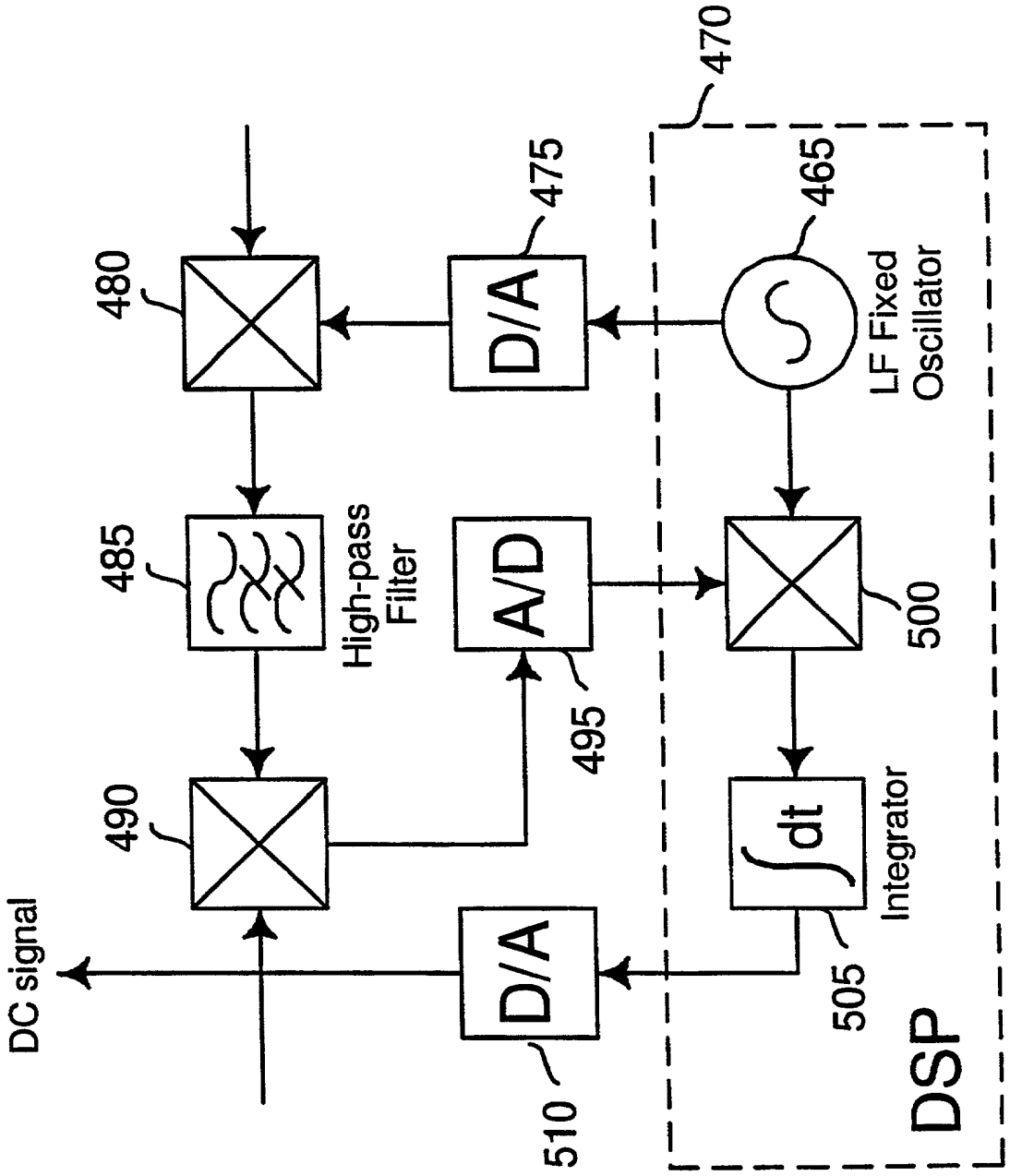
470
475
465
480
D/A
LF Fixed Oscillator
485
High-pass Filter
A/D
500
495
490
dt
Integrator
DC signal
D/A
505
510
DSP

Fig. 4

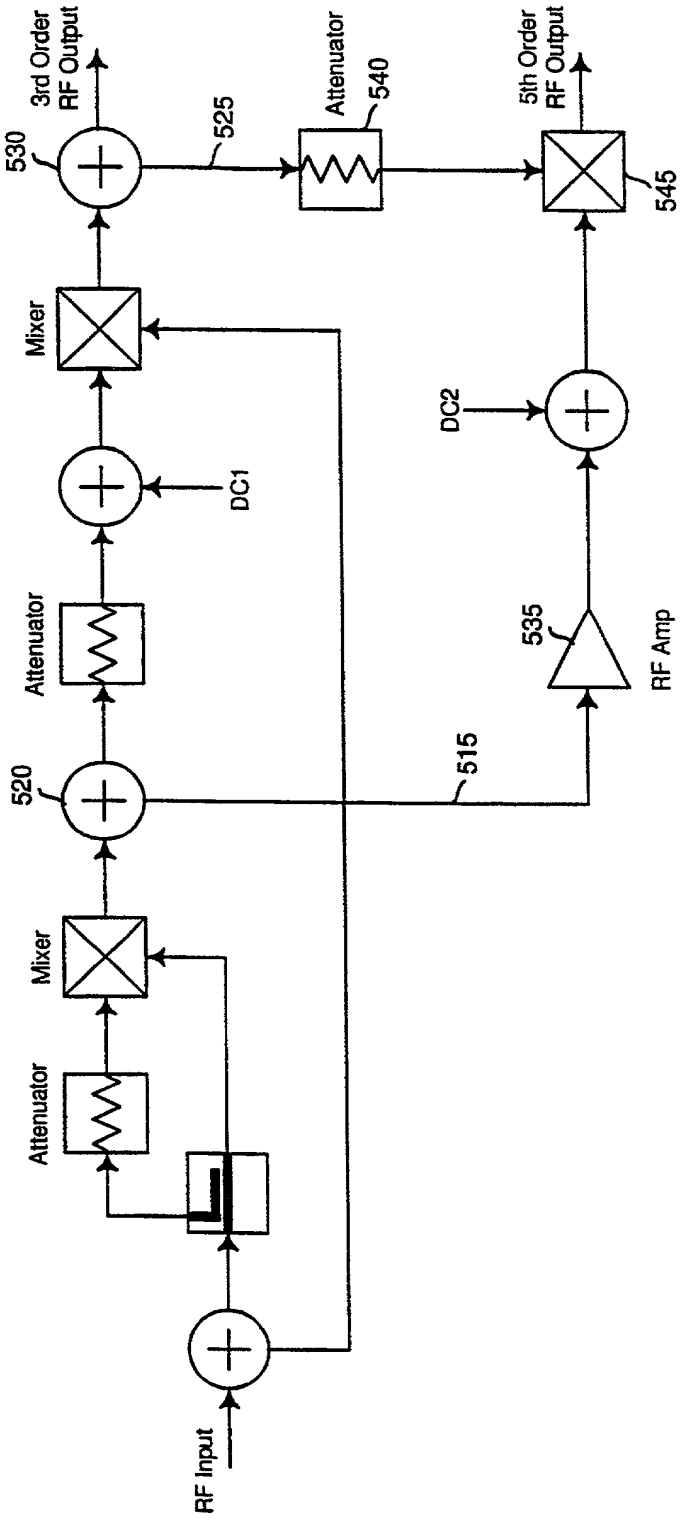
3rd Order RF Output
530
525
Attenuator
540
5th Order RF Output
545
Mixer
DC2
DC1
Attenuator
535
RF Amp
520
515
Mixer
Attenuator
RF Input

Fig. 5

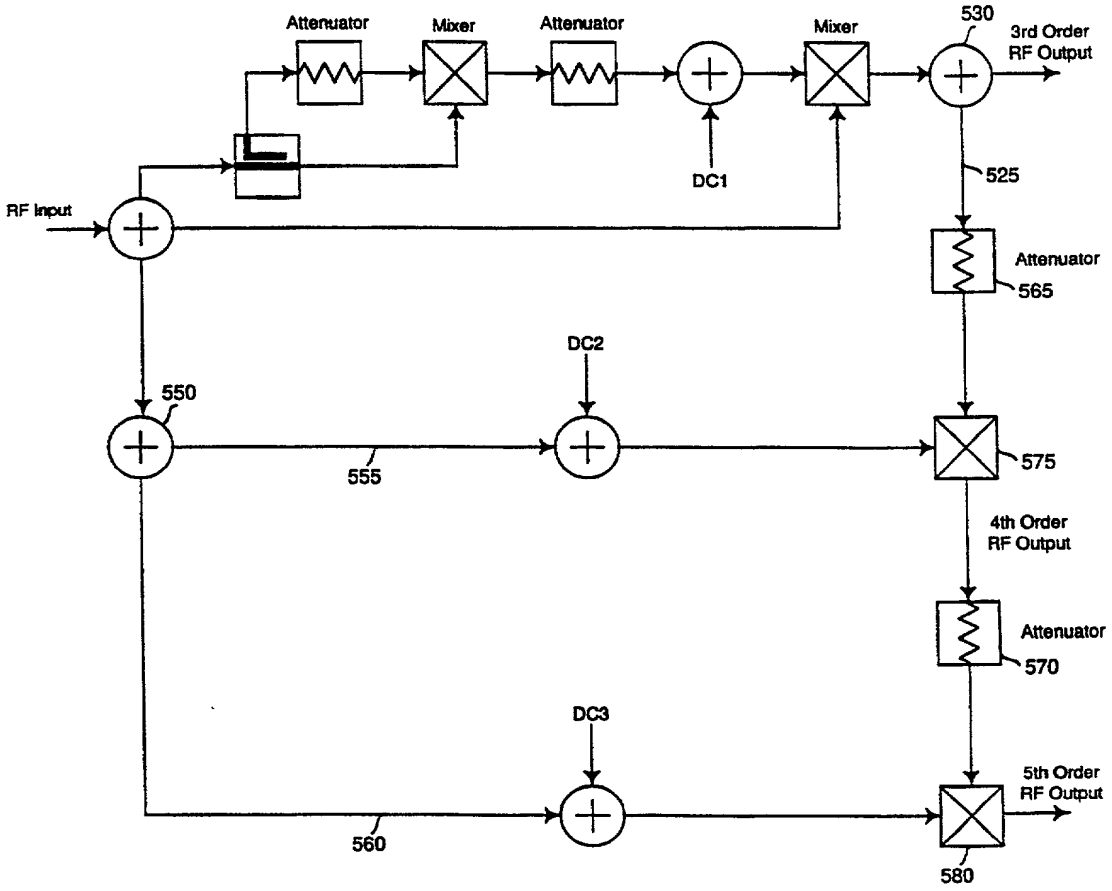
Attenuator
Mixer
Attenuator
Mixer
530
3rd Order
RF Output
DC1
525
RF Input
Attenuator
565
DC2
550
555
575
4th Order
RF Output
Attenuator
570
DC3
5th Order
RF Output
560
580

Fig. 6

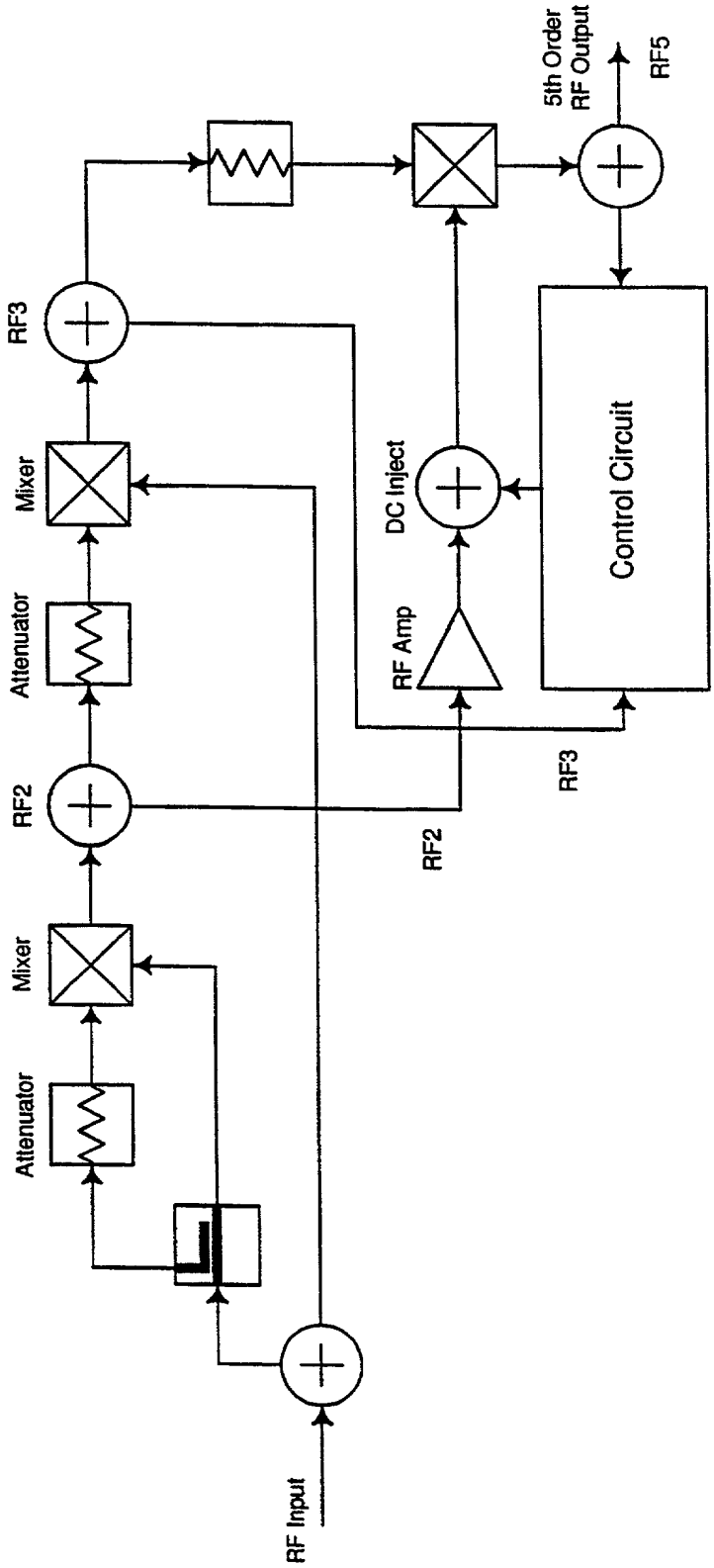
5th Order
RF Output
RF5
RF3
Mixer
Attenuator
RF2
Mixer
Attenuator
RF Input
DC Inject
RF Amp
Control Circuit
RF3
RF2

Fig. 7

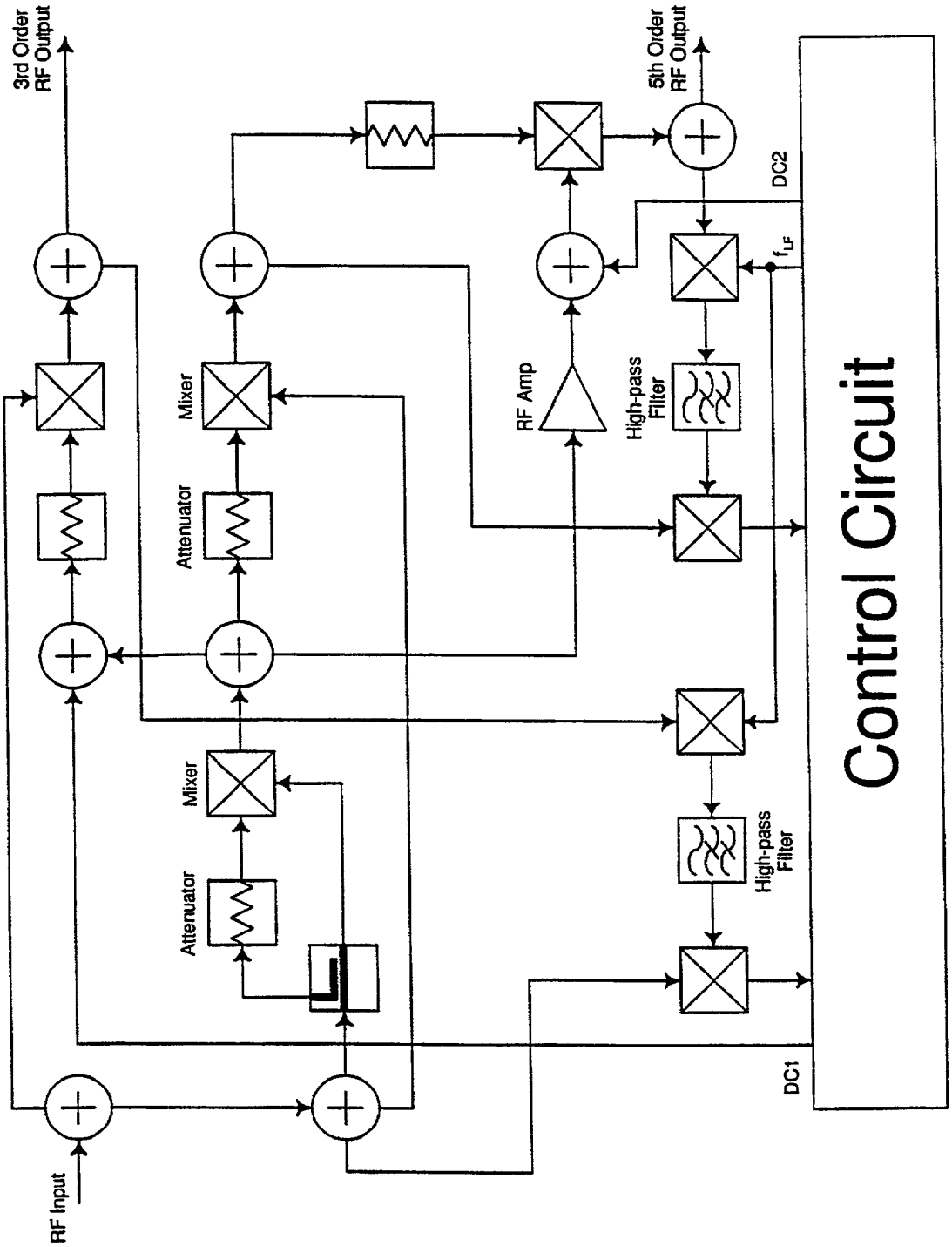
3rd Order RF Output
5th Order RF Output
DC2
f_{LF}
RF Amp
High-pass Filter
Mixer
Attenuator
Mixer
Attenuator
High-pass Filter
Control Circuit
DC1
RF Input

Fig. 8

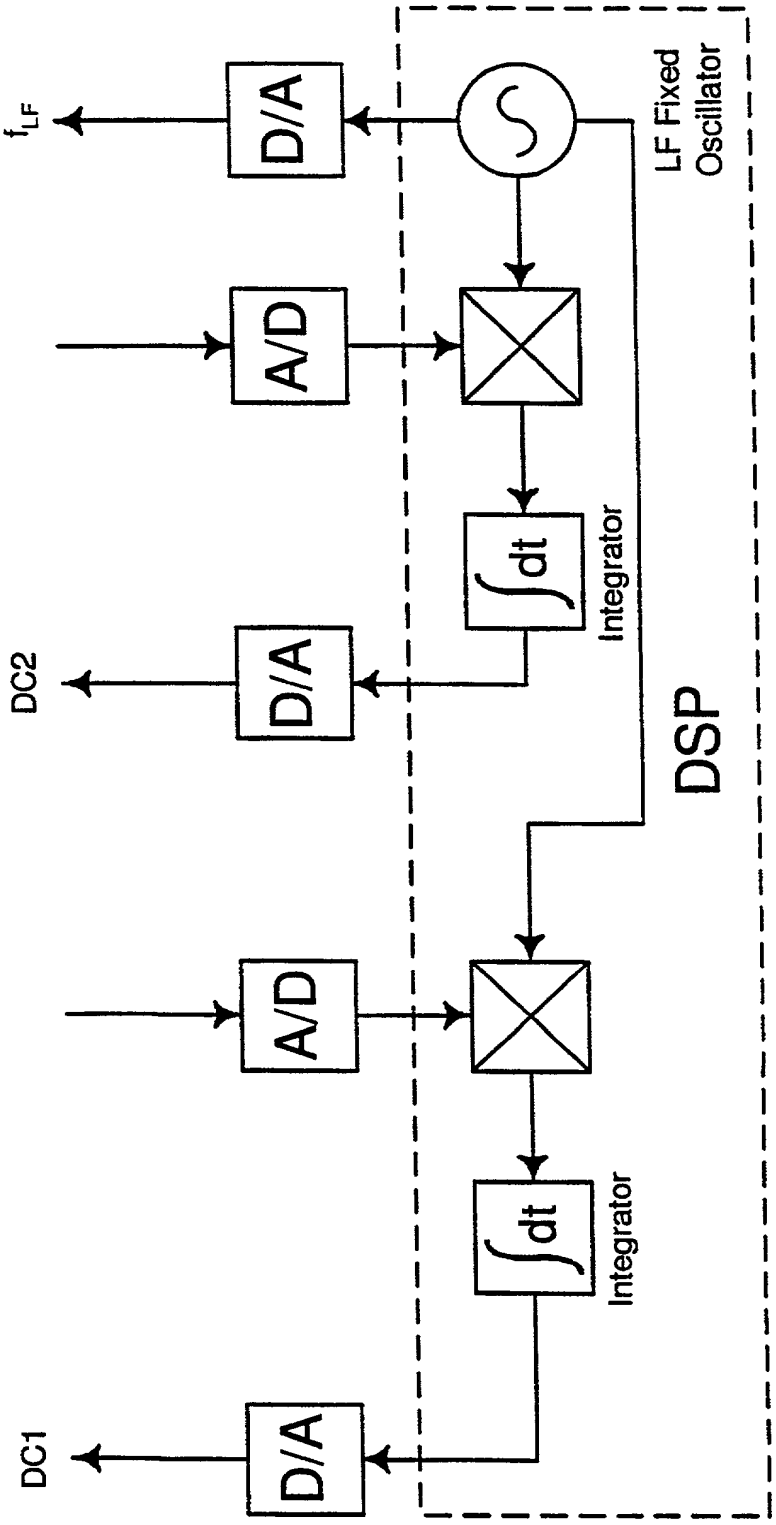
f_{LF}
D/A
LF Fixed Oscillator
A/D
$\int dt$
Integrator
DC2
D/A
DSP
A/D
$\int dt$
Integrator
DC1
D/A

Fig. 9

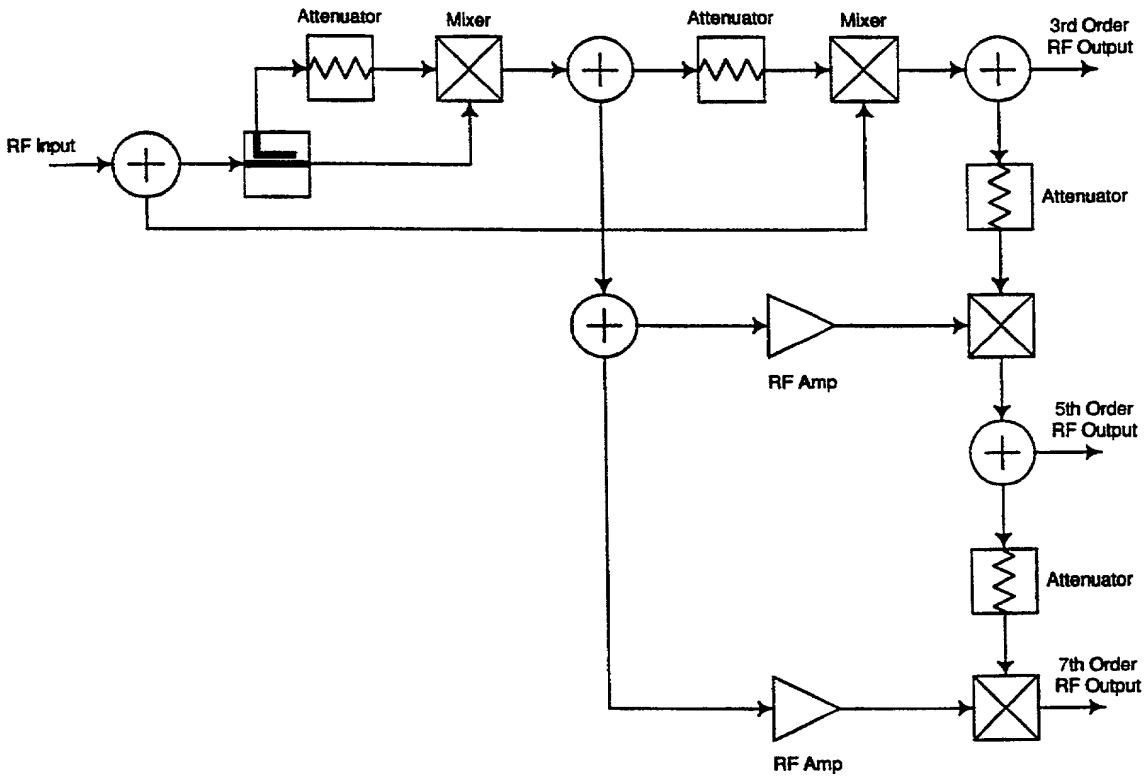
Attenuator
Mixer
Attenuator
Mixer
3rd Order
RF Output
RF Input
Attenuator
RF Amp
5th Order
RF Output
Attenuator
7th Order
RF Output
RF Amp

Fig. 10

Fig 11a

Fig 11b

Fig 11c

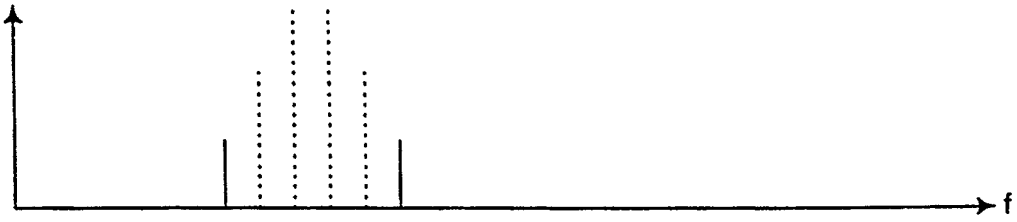

Fig 11d

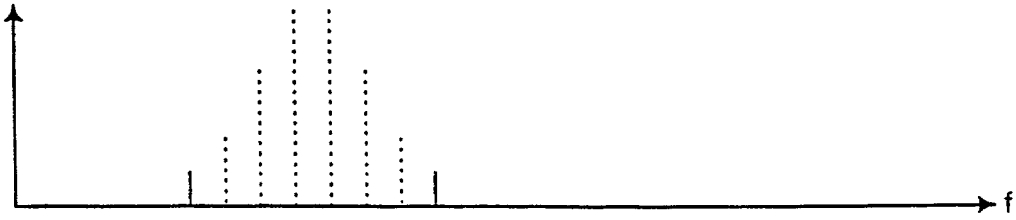

Fig 11e

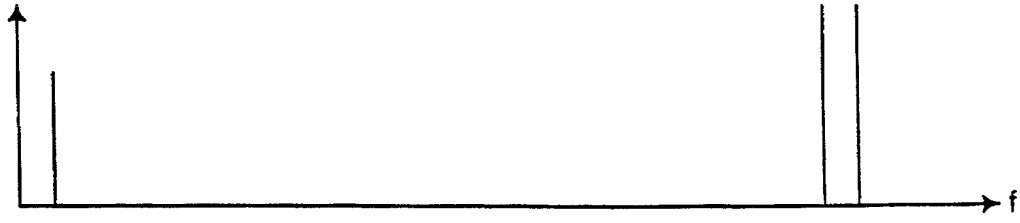

Fig 11f

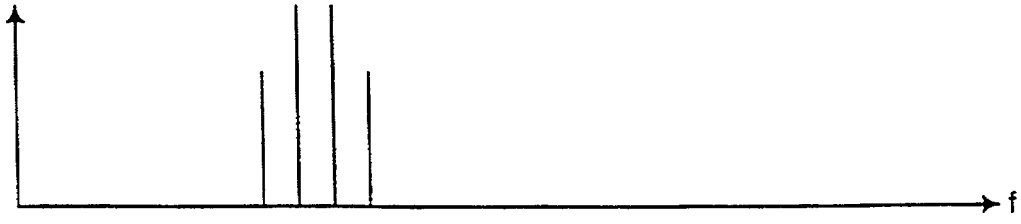

Fig. 11

FOR UTILITY PATENT APPLICATION 37 C.F.R. § 1.63		Attorney Docket No.	46387/247138
		First Named Inventor	Peter Kenington
		COMPLETE IF KNOWN	
Declaration submitted with initial filing	Declaration submitted after Initial Filing (Surcharge (37 CFR 1.16(e)) required)	Application Number Filing Date Group Art Unit Examiner Name	09/623,646 09/06/2000 September 6, 2000 5001 Christine S. Washington

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PREDISTORTER

the specification of which (check only one item below):

is attached hereto

was filed as United States Application Serial No.
and was amended on _____ (if applicable).

was filed as PCT International Application Number PCT/GB99/00695 on
March 8, 1999 and was amended under PCT Article 19 on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or any PCT international application having a filing date before that of the application(s) on which priority is claimed:

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Claimed		Certified Copy Attached?	
9804745.9	U.K.	03/06/1998	YES	NO	YES	NO
		(March 6, 1998)	YES	NO	YES	NO
			YES	NO	YES	NO
			YES	NO	YES	NO
			YES	NO	YES	NO

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s) or PCT international application(s) designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

U.S. APPLICATIONS		STATUS (Check One)		
U.S. Application Number	U.S. Filing Date (MM/DD/YYYY)	Patented	Pending	Abandoned
PCT APPLICATIONS DESIGNATING THE U.S.				
PCT Application No.	PCT Filing Date	U.S. Serial Numbers Assigned (if any)		

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(List name and registration number)*

John S. Pratt 29,476; Anthony B. Askew 24,154; Roger T. Frost 22,176; Robert E. Richards 29,105; James L. Ewing, IV 30,630; Stephen M. Schaetzel 31,418; Charles W. Calkins 31,814; Larry A. Roberts 31,871; James Dean Johnson 31,771; Jamie L. Greene 32,467; George T. Marcou 33,014; Dean W. Russell 33,452; Richard T. Peterson 35,320; Charles T. Simmons 35,359; Nora M. Tocups 35,717; Bruce D. Gray 35,799; Theodore R. Harper 35,890; Geoff L. Sutcliffe 36,348; Leona G. Young 37,266; Suzanne Seavello Shope 37,933; Mitchell G. Stockwell 39,389; Mary Anthony Merchant 39,771; Brenda Ozaki Holmes 40,339; Michael J. Turton 40,852; Kimberly J. Prior 41,483; J. Steven Gardner 41,772; Theodore M. Green 41,801; James J. Bindseil 42,326; Richard H. Lilley 42,803; John K. McDonald 42,860; Sima Sinadia Kulkarni 43,732; Camilla C. Williams 43,992; Christopher J. Chan 44,070; Carl B. Massey; 44,224; R. Whitney Winston 44,432; John William Ball, Jr. 44,433; John M. Briski 44,562; S. Craig Hemenway 44,759; Kristin L. Johnson 44,807; Paul E. Knowlton 44,842; Charles E. Peeler 45,004; Bambi F. Walters 45,197; Cheryl L. Huseman 45,392; Shelby B. Grier 45,785; Vaibhav P. Kadaba 45,865; Donald R. Andersen 28,280; Kyle M. Globerman 46,730; Tywanda L. Harris 46,758; Kristin D. Mallatt 46,895; Joseph Bennett-Paris 47,226

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Send Correspondence to:	John S. Pratt, Esq. Kilpatrick STOCKTON LLP 1100 Peachtree Street, Suite 2800 Atlanta, GA 30309-4530 Phone: (404) 815-6367 Fax: (404) 815-6555	Customer No. 23370

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statement may jeopardize the validity of the application or any patent issuing thereon.

Name of Sole or First Inventor:	Peter Kenington		
Inventor's Signature and Date:	P.R. Kenington	Date: 6th FEB 2001	
Residence Address and Citizenship:	Chepstow, United Kingdom GBR	Citizenship	U.K.
Post Office Address:	Trap Farm, Devauden Green, Chepstow NP6 6PE, United Kingdom		